

CLAIMS

What is claimed is:

1. A memory module comprising:
2. a plurality of memory devices; and
3. a memory module controller configured to receive a memory
4. transaction from a first memory bus and to control access to the plurality of
5. memory devices.

1 2. The memory module of claim 1, wherein the memory module
2 controller receives the memory transaction in a first format and reformats the
3 memory transaction into a second format, the memory module controller
4 providing the reformatted memory transaction to at least one of the plurality
5 of memory devices.

1 3. The memory module of claim 1, further comprising a second memory
2 bus coupled between the memory module controller and the plurality of
3 memory devices.

1 4. The memory module of claim 3, wherein the second memory bus
2 comprises separate address, data, and control signal lines.

1 5. The memory module of claim 1, wherein the second memory bus
2 comprises a clock signal.

1 6. The memory module of claim 1, wherein the first memory bus
2 operates at a first data rate and the second memory bus operates at a second
3 data rate, wherein the first data rate is different than the second data rate.

1 7. The memory module of claim 1, wherein the first memory bus has a
2 first number of signals lines and the second memory bus has a second
3 number of signal lines, wherein the first number of signal lines is different
4 than the second number of signal lines.

1 8. The memory module of claim 1, wherein the memory module
2 controller comprises:

3 request handling circuitry structured to receive the memory
4 transaction from the first memory bus; and

5 control logic coupled to the request handling circuitry and reformatting
6 the memory transaction, the memory module controller providing the
7 reformatted memory transaction to at least one of the plurality of memory
8 devices.

1 9. The memory module of claim 1, wherein the first memory bus carries
2 time-multiplexed data and address information, and the second memory bus
3 includes separate address and data lines.

1 10. The memory module of claim 1, wherein the memory module is a
2 dual in-line first memory module (DIMM).

1 11. The memory module of claim 1, wherein the memory module is a
2 single in-line first memory module (SIMM).

1 12. The memory module of claim 1, wherein the plurality of memory
2 devices comprise volatile memory devices.

1 13. The memory module of claim 1, wherein the plurality of memory
2 devices comprise nonvolatile memory devices.

Sub 3

1 14. The memory module of claim 1, wherein the memory module
controller generates a handshake signal that indicates when the memory
3 module controller is communicating data to the system memory controller.

1 15. The memory module of claim 1, wherein the memory transaction is a
2 write transaction.

1 16. The memory module of claim 1, wherein the memory transaction is a
2 read transaction.

1 17. A memory module comprising:
2 a plurality of memory devices; and
3 a memory module controller coupled to a plurality of memory devices,
4 wherein the memory module controller receives a first memory transaction
5 from the memory bus in a first format and provides a second memory
6 transaction in a second format to at least one of the second plurality of
7 memory devices.

Add C1 >